Synopsys Timing Constraints And Optimization User Guide

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Synopsys Timing Constraints And Optimization

Synopsys Timing Constraints and Optimization User Guide
Synopsys® Timing Constraints and Optimization User Guide Version D-201003, March 2010
A Power-Centric Timing Optimization Flow - Synopsys
– Available now via SolvNet for joint Synopsys and ARM customers 1 “big” cluster: dual-core Cortex-A15 processor – Scripts, design information, documentation
DC Ultra - Synopsys
synopsyscom Overview • Concurrent optimization of timing, area, power and test prioritizes design rule requirements over timing and area constraints By setting the appropriate priority, designers can drive synthesis to achieve the best QoR for a design Compile directives in DC Ultra can be used to further control optimization
Automated Synthesis from HDL models
Automated Synthesis from HDL models Design Compiler (Synopsys) Leonardo (Mentor Graphics) Design optimization constraints: user-specified timing and area optimization goals DC tries to optimize these without violating design rules Common constraints: timing and area
Using the Synopsys Design Constraints Format Application ...
Using the Synopsys Design Constraints Format 1 Synopsys Design Constraints (SDC) is a format used to specify the design intent, including the timing, power, and area constraints for a design SDC is based on the tool command language (Tcl) The Synopsys Design Compiler, IC Compiler, and PrimeTime tools use the

RTL-to-Gates Synthesis using Synopsys Design Compiler

meet timing and ultimately fail If the period is too large, then the tools will have no trouble but you will get a very conservative implementation For more information about constraints consult the Synopsys Timing Constraints and Optimization User Guide (dc-user-guide-tcopdf) dc_shell> create_clock clk -name ideal_clock1 -period 2

RTL-to-Gates Synthesis using Synopsys Design Compiler

Synopsys Design Compiler to elaborate RTL, set optimization constraints, synthesize to gates, and prepare various area and timing reports You will also learn how to read the various DC text reports and how to use the graphical Synopsys Design Vision tool to visualize the synthesized design

Design Compiler Register Retiming Reference Manual

retiming performs a sequential optimization that moves registers to optimize timing and area It optimizes gate-level netlists to meet timing while trying to use as few registers as possible This manual supports the Synopsys synthesis tools, whether they are running under the UNIX operating system or the Linux operating system

Synopsys FPGA Synthesis

Synopsys FPGA Synthesis Synplify Pro Tutorial March 2010 chical Optimization Technology, High -performance ASIC Prototyping System, HSIM, HSIMplus, i-Virtual Stepper, IICE, timing constraints The constraint file will be created using this tutorial However, you can

Design Constraints User's Guide

Timing Constraints Timing constraints represent the performance goals for your designs Designer software uses timing constraints to guide the timing-driven optimization tools in order to meet these goals You can set timing constraints either globally or to a specific set of paths in your design You can apply timing constraints to:

Xilinx Synopsys Interface EPLD User Guide

Synopsys Design Compiler Timing and resource utilization results are available from XEPLD after completion of fitting (fitnet) The XEPLD fitter (v50) currently does not support timing-constraint-driven optimization; Synopsys timing constraints have no effect on …

RTL-to-Gates Synthesis using Synopsys Design Compiler

use Synopsys Design Compiler to elaborate RTL, set optimization constraints, synthesize to gates, and prepare various area and timing reports Synopsys provides a library called Design Ware which includes highly optimized RTL for arithmetic building blocks For example, the Design Ware libraries contain adders, multipliers, comparators, and

RTL-to-Gates Synthesis using Synopsys Design Compiler

divisor (GCD) cicruit, set optimization constraints, synthesize the design to gates, and prepare various area and timing reports You will also learn how to read the various DC text reports and how to use the graphical Synopsys Design Vision tool to visualize the synthesized design Note that this tutorial is by no means comprehensive

Quartus II Handbook Volume 2: Design Implementation and …

User-created constraints are contained in one of two files: the Quartus II Settings File (qsf) or, in the case of timing constraints, the Synopsys Design Constraints file (sdc) Constraints and assignments made with the Device dialog box, Settings dialog box, Assignment Editor, Chip Planner, and Pin

HSPICE User Guide, RF Analysis

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Design Constraints User Guide

The Libero SoC software supports both SDC timing and PDC physical constraints In addition, it supports netlist optimization constraints You can set constraints by either using Microsemi's interactive tools (I/O Editor, Chip Planner, and Constraint Editor) or by

PrimeTime Advanced Timing Analysis User Guide

PrimeTime® Advanced Timing Analysis User Guide Version F-201112, December 2011

Synopsys Low-Power Flow User Guide

Synopsys Low-Power Flow User Guide F-201109Synopsys Low-Power Flow User Guide Version F-201109 What’s New in This Release The Eclypse™ Low Power Solution is a comprehensive portfolio of Synopsys tools that

Hierarchical Design Using Synopsys and Xilinx FPGAs

Hierarchical Design Using Synopsys and Xilinx FPGAs By: Kate Kelley 2 wwwxilinxcom WP386 (v10) February 15, 2011 timing constraints for each compile point block partition boundary from being critical because there is no logic optimization across boundaries If it is not possible to register both inputs and outputs, it is